Modeling Simultaneous Switching Noise-Induced Jitter for System-on-Chip Phase-Locked Loops

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ABSTRACT

Phase-Locked Loops (PLLs) are versatile modules for synchronization and applications such as high-speed serial interfaces in System-on-Chips (SoCs). Their precisions are critical to proper functioning of the SoCs. Intermodule interference such as simultaneous switching noise (SSN) is time-varying, where the stationary assumption in conventional jitter analysis does not apply. We propose a methodology to compute PLL jitter by investigating the harmonic relations between the PLL system with SSN. This provides statistical analysis over many VCO design parameters, SoC modules and noise barrier configurations. Its accuracy and efficiency are compared against circuit simulations.

Categories and Subject Descriptors

B.7.2 [**Integrated Circuits**]: Design Aids; I.6.5 [**Model Development**]: Modeling Methodologies

General Terms

Algorithms, Performance

Keywords

Phase-locked loop, Jitter, Switching noise, Cyclostationary

1. INTRODUCTION

S*ystem-on-chip* (SoC) integrates an entire system onto a common silicon die. To realize the full benefits of system integration, intermodule interference associated with increased clock rate and diminished modular separation distances must first be overcome. *Phase-locked loop* (PLL) is a common subsystem in the SoC architecture for synchronization and frequency synthesis in high-speed applications, such as clock and data recovery (CDR) at serial interfaces. Due to the increase in the number of clock domains and data interfaces, there is a tendency to populate complex SoCs with multiple PLLs. The quality of a PLL is vital to ensure proper system operations. It is determined by the lock range and precision of its oscillation frequency, with the latter measured by the time interval between threshold-crossings of its oscillating output, given an *ideal* reference frequency source. The short-term variations of this interval from its mean value is known as *timing jitter,* or simply *jitter*. Traditional PLL jitter analysis focuses solely on *stationary intrinsic* noise emanated from its internal devices [1]. External interference, such as power supply noise and substrate coupling are now prevalent in SoCs [2]. They arise due to consequences of impulsive charge injection during gate switching, hence commonly known as *simultaneous switching noise* (SSN).

SSN is distinguished from stationary intrinsic device noise by its temporal *correlation* with the PLL. Transient pulses with distinctive *signatures* and *periodicities* are emitted from the sea of switching digital gates. The exhibited noise signatures are dictated by the specific combination of the states of the neighboring circuits. Its periodicities and power spectra are related to the PLL power spectrum, as nearby SSN sources are usually driven by signals derived from the PLL. This temporal correlation may render SSN more detrimental to PLL performance than stationary noise, since the ambient noise level constantly changes at rates much faster than the response time of the PLL feedback control loop. In this paper, we present a methodology to describe the statistical jitter contributed by SSN. First, *cyclostationary SSN* models are extracted from sample noise signatures from various *clock domains*, using the *Karhunen-Loeve* expansion [3] method. It is an optimal linear transformation that reduces high-dimensionality datasets while maintaining the resultant subspace with the largest variances. The periodic (linear) time-varying noise sensitivity of the PLL is then derived. Finally, parasitic coupling paths leading to the PLL are identified and used to compute the jitter induced by SSN.

2. BACKGROUND

A typical integrated PLL consists of a *voltage-controlled oscillators* (VCOs) and a feedback control circuit. Due to the ease of integration and low-*Q*, low gain limitations, *ring oscillator* (RO) VCOs are preferred in CMOS SoCs over *tuned LC circuits* and *relaxation oscillators*. The VCO oscillation frequency is dictated by a control voltage, regulated by the control loop. It acts to compensate for the phase differences between the PLL output and a reference signal. In its steady-state locked to a reference signal, an *ideal* PLL output signal can be represented by a periodic voltage $v(t)$. In practice, the steady-state mean-square jitter of a PLL waveform is non-zero. Its Fourier series expansion can thus be expressed as

$$v(t) = \sum_{n=-\infty}^{\infty} A_n \exp\left(jn\left(\frac{2\pi t}{T_0} - \phi(t)\right)\right), \quad (1)$$

where $\phi(t)$ denotes the *phase lag*, or *phase noise,* due to interference and non-idealities, accumulated from all previous oscillation cycles. Fig. 1 shows the propagation of $\phi(t)$ in a linear PLL model. Even when $v(t)$ is relatively noise-free, $\phi(t)$ is non-zero and accumulates until it is sensed by the *Loop Filter* (LF) and eventually corrected by altering $v(t)$. The loop filter is a low-pass filter that has a lower bandwidth than the VCO (typi-

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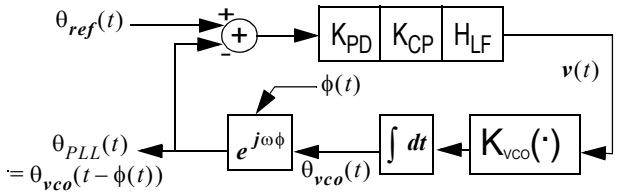

Fig. 1 Ring oscillator PLL linear model

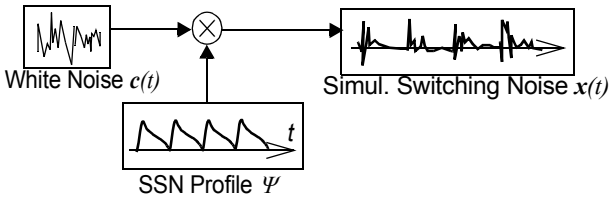

Fig. 2 Equivalent model of SSN generation from noise profiles derived from substrate coupling simulations

cally $1/20^{th}$ to $1/100^{th}$). During the initial tens of cycles, $\phi(t)$ is passed to the PLL output unregulated by the feedback loop. For instance, suppose a CDR circuit driven by a PLL is interfered by SSN, with comparable periodicity as the PLL. As the PLL locks onto the phase of the incoming data signal, its transition is skewed by SSN, creating jitter. Due to the low-pass nature of LF, the feedback mechanism typically requires a few tens of cycles to compensate for the jitter. At the next PLL cycle, a new group of SSN pulses of *different* intensity arrives before this jitter is effectively eliminated. This cycle-to-cycle statistical variations renders the feedback mechanism inefficient. As long as the SSN fundamental frequency is much less than the LF bandwidth, short-term SSN-induced PLL jitter is largely determined by the jitter in the VCO, or $\phi(t) \approx \phi_{vco}(t)$. Let t_2 be the elapse time for $v(t)$ in (1) to complete N VCO periods T_0 since t_1, or $t_2 - t_1 = NT_0 + \Delta t$, where Δt is the *timing jitter*. It can be expressed in terms of absolute time or per unit interval (*UI*). Factors contributing to $\phi_{vco}(t)$ arise from its *intrinsic* device noise, such as thermal, shot, flicker noise, or from various *external* sources, such as signal line crosstalk, power supply noise, well and substrate coupling. From (1),

$$\begin{cases} 2\pi t_1/T_0 - \phi(t_1) = t_0 \\ 2\pi t_2/T_0 - \phi(t_2) = t_0 + 2\pi N \end{cases} \quad (2)$$

Taking the difference of the equation pair, the total timing jitter between time t_1 and t_2 is

$$\Delta t(t_1, t_2) = \frac{T_0}{2\pi}(\phi_2 - \phi_1), \quad (3)$$

where $\phi_i = \phi(t_i)$. The *mean square* timing jitter is

$$\langle \Delta t^2(t_1, t_2) \rangle = \frac{T_0^2}{4\pi^2}(R_{\phi_1\phi_1} + R_{\phi_2\phi_2} - 2R_{\phi_1\phi_2}), \quad (4)$$

where R is the *autocorrelation* function of $\phi(t)$. Suppose intrinsic and external noise components are additive, we propose that $\phi(t)$ is contributed by (*i*) *stationary* and (*ii*) *cyclostationary* noise sources in SoC environments. Much work [1,4] has been devoted to analyze jitter due to the first type. In the following sections, we compute the jitter component induced by the cyclostationary noise in SoCs. We refer the SSN-induced jitter component simply as *jitter* from this point on unless stated otherwise.

3. SSN MODEL GENERATION

In the mixed-signal environment, function blocks are integrated in close proximity to share the power supply and substrate. Simultaneous switching noise (SSN) is the collective charge coupling generated by large number of digital gates switching synchronously. Increased device density, packaging parasitics and low substrate resistivity deteriorate the electrical isolation among subsystems. For instance, average transient peaks of global chip substrate potentials in excess of 0.1V are common for million-transistor digital circuits. SSN affects normal system operation by varying delay characteristics and junction potentials of transistors. To ensure that designers provide adequate performance margin, good estimation of chip-level SSN coupling are needed. It is determined by:

1. Signature and magnitude of SSN sources,
2. Parasitic values of coupling paths, and
3. Noise sensitivity of target circuitry.

In this section, we propose a compact SSN model that characterizes the noise signatures from data samples. The coupling path parasitics and the VCO noise sensitivity will be derived in section 4 to obtain the SSN-induced jitter.

3.1 Cyclostationarity

SSN is stochastic, periodic and with the majority of activities concentrated in certain short intervals relative to the clock transitions. An example of the substrate coupled SSN observed at the bulk substrate beneath the VCO is shown in Fig. 3(a). In clock distribution networks, this switching noise source is highly related to the VCO transitions. To obtain accurate SSN waveforms without costly simulation of large circuits, we propose a compact *cyclostationary* model that captures the distinctive *noise profile* $\boldsymbol{f}(t)$ from SSN samples derived from simulations, where complete periods of SSN samples are weighted by their occurence probabilities. Suppose a SSN period spans P simulation time steps, the i^{th} period of model-generated SSN $x(t)$ is given by

$$[x_{i1}, \ldots, x_{iP}]^t = \sum_{j=1}^{N} c_{ij}\psi_j(t) = \Psi \boldsymbol{c}_i. \quad (5)$$

$\boldsymbol{c}_i = [c_{i1}, \ldots, c_{iN}]^t$ is a column vector of *uncorrelated* normally-distributed coefficients. (5) implies that $x(t)$ is generated periodically by $\boldsymbol{f}(t) \equiv \Psi$ and N *stationary* Gaussian weights $\boldsymbol{c}_i$ as depicted in Fig. 2. We shall now show the derivation and reduction of the optimum basis Ψ for *cyclostationary* process using *Karhunen-Loeve* (KL) Expansion.

3.2 The Karhunen-Loeve Basis

The SSN basis Ψ in (5) is a $P \times N$ matrix $[\psi_1(t), \ldots, \psi_N(t)]$ denoting the column space of a set of N basis functions. It suffices for Ψ to be of full column rank, i.e. $N \le P$. Detail derivation of the optimum Ψ using the *Karhunen-Loeve* (KL) method is shown in Subsection *7.1*. Example of the KL basis derived from SSN samples is shown in the inset figure in Fig. 3(a). A funda-

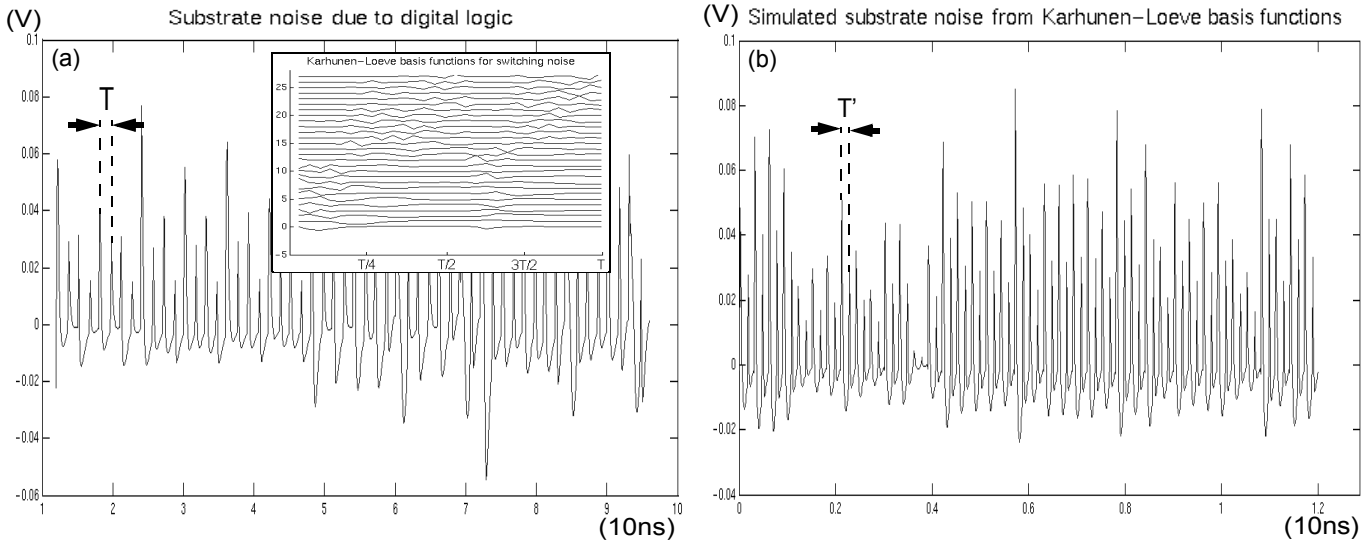

Fig. 3 (a) Substrate coupling due to digital logic switching activities, its KL basis functions, and (b) KL model-generated noise

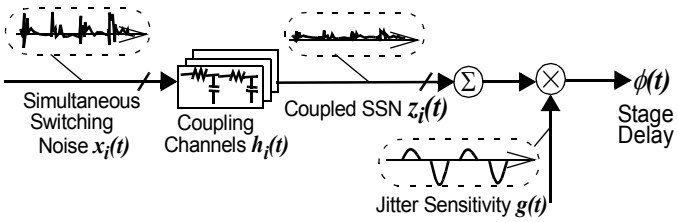

Fig. 4 Noise-to-jitter transfer model

mental property of KL expansion is that it is the optimal linear transformation that identifies orthogonal basis functions that maximize the variances of the dataset when projected on them. For *partial* basis expansions in particular, it aligns them along the data in the most interesting dimensions. Only a few basis functions are often needed to adequately capture any given SSN signature, providing a compact and high-resolution model.

If the basis functions are sorted with the largest corresponding eigenvalues first, this ordered KL expansion gives the most accurate representation for a reduced number (usually <10) of basis functions by retaining the first few *principal* components and truncate the rest. Using $N \ll P$ principal components in (5) reproduces a *statistically identical* SSN time sequence of arbitrary length at minimal computation cost

$$x(t) = x(t' + kT_f) = \boldsymbol{f}(t')\boldsymbol{c}\,, \qquad t' \in [0, T_f)\,, \tag{6}$$

where k is an integer, $\boldsymbol{f}(t') = [\psi_1(t'), \psi_2(t'), \ldots, \psi_N(t')]$, and $\boldsymbol{c} = [c_1, c_2, \ldots, c_N]^t$. $c_1, c_2, \ldots$ are random scalar coefficients drawn from its corresponding distribution every period. The new SSN waveform can be easily scaled to investigate its relation to the PLL frequency. An example of $x(t)$ using 10 basis functions is shown in Fig. 3(b).

4. SSN-INDUCED JITTER

The SSN from multiple clock domains is represented by model-generated SSN samples, and coupled to the PLL simultaneously according to the model illustrated in Fig. 4 through their specific parasitic pathways, such as the substrate, *n*-well bias networks, ground or power supply connections.

4.1 Coupling Paths and Jitter Sensitivities

Parasitic coupling paths for each SSN source are established via a parasitic extraction scheme. Each $x_i(t)$ and $h_i(t)$ in Fig. 4 correspond respectively to a SSN source and the impulse response of its coupling path, contribute to the SSN perceived by the VCO. $g(t)$ is its *jitter sensitivity*. In particular, due to well bias junction capacitances, *p*MOS in *n*-wells are more insulated from SSN coupling than the *n*MOS in the bulk substrate. As SoC performance is sensitive to interconnect coupling, particularly noisy SSN sources and high conductivity paths must be identified as early as possible in the design flow.

In typical design flows, detailed layout geometry is often not available until after the schematic design is finalized. Instead, estimation of coupling paths $h_i(t)$ can be constructed based on material properties, block separation distances and parasitic conductivities. For substrate coupling, epitaxial and bulk conductivities and geometric distances among the geometric centroids of the digital blocks and the VCO are used. *n*-well devices body connections can also be derived from their direct distances to their doping tubs bias nodes. Coupling across the power supply nets can be modeled the similarly based on wire length.

The following section explores the effects of the relative phase and frequency differences among $x_i(t)$ and $g(t)$. In our following development of the jitter equation, we represent functions in the continuous time domain to avoid the additional confusions of the multiple sampling frequencies for each time function. The discrete time equivalence of the final equation will given in the numerical implementation section.

4.2 Computation of SSN-Induced Jitter

In clock generation and synchronization applications, the number of delay elements in the ring and their individual propagation delays are important design parameters affecting its precision

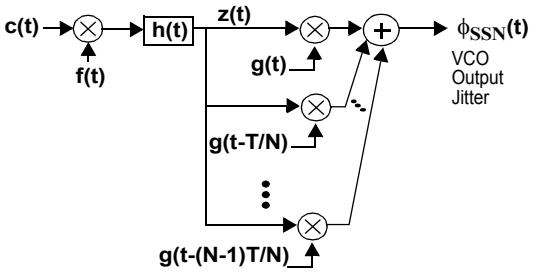

Fig. 5 *N*-stage ring oscillator output jitter model

and operable frequency range. Suppose an oscillator has a ring connection of n delay elements. We model the *instantaneous phase lag* of *one* infected delay element (together with $n-1$ noiseless elements) due to SSN coupling as

$$\varphi(t) = [h(t)*x(t)]g(t) = \int_{-\infty}^{t} h(t-\tau)\boldsymbol{f}(\tau)\boldsymbol{c}d\tau \cdot g(t) . \qquad (7)$$

$g(t)$ is the time-varying noise sensitivity of one stage of the ring oscillator (RO). It is periodic with oscillator period T_g and thus has discrete Fourier expansion $\sum_{n=-\infty}^{\infty} G_n \exp(j2\pi nt/T_g)$. Assuming an *N*-stage inverter (differential amplifier) RO, sharing identical delay and parasitic characteristics, there are n falling and n rising transitions in each period. For CMOS inverters, the falling and rising transitions are sensitive to substrate and *n*-well coupled noise respectively, while for differential amplifiers, both transitions types are sensitive to coupled SSN. The instantaneous jitter model for differential amplifiers RO is shown in Fig. 5. The coupled noise $z(t)$ is sampled at N evenly-distributed instances per period. The *instantaneous* jitter due to SSN is thus of the N time-shifted sensitivity functions super-imposed

$$\varphi(t) = \int_{-\infty}^{t} h(t-\tau)\boldsymbol{f}(\tau)\boldsymbol{c}d\tau \cdot \sum_{l=0}^{N-1} g\left(t-\frac{lT_g}{N}\right). \qquad (8)$$

To explore the temporal correlations between the SSN and PLL noise sensitivity, we expand the spectra of $\boldsymbol{f}(t)$ and $g(t)$. $x(t)$ is projected onto its partial KL basis in (6). To show its interactions with $g(t)$, (6) is projected onto the complex exponential basis

$$x(t) = \boldsymbol{e}^t \Psi \boldsymbol{c} = \sum_{m=-\infty}^{\infty} \sum_{i=1}^{N} \Psi_{im} c_i \exp\left(\frac{j2\pi m\tau}{T_f}\right), \qquad (9)$$

where $\Psi_{im} = 1/T_f \int_{T_f} \psi_i(\tau)\exp(j2\pi m\tau/T_f)d\tau$, T_f is the SSN period. Let $\boldsymbol{F}_m = [\Psi_{1m}, \Psi_{2m}, \ldots, \Psi_{Nm}]$, the instantaneous phase lag becomes $\varphi(t) = \sum_{m,r=-\infty}^{\infty} A_{m,r}\exp\left(j2\pi t\left(\frac{rN}{T_g}+\frac{m}{T_f}\right)\right)$, (10)

where $A_{m,r} = NH_m\boldsymbol{F}_m\boldsymbol{c}G_{rN}$. Refer to Subsection *7.2* for derivation details of (10). The phase noise at the i^{th} transition is the integral of $\varphi(t)$ to the current transition time

$$\phi[i] = \phi(iT_g) = \int_0^{iT_g} \varphi(t)dt \text{, while } \phi[i] \ll iT_g . \qquad (11)$$

For the most accurate treatment, the end time of integral (11) should be taken as exact current time with jitter, i.e. $iT_g + \phi[i]$. However, $\phi[i]$ has to be solved at each time step iteratively. Instead, for $\phi[i] \ll iT_g$, (11) is simplified to integrate up to iT_g in order to give an approximated analytical solution.

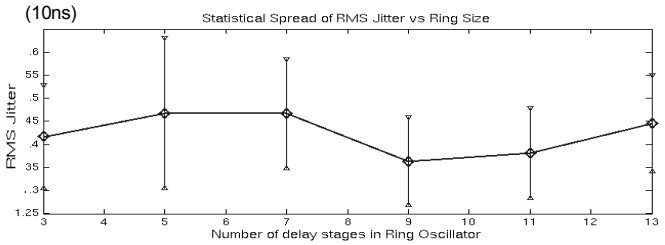

Fig. 6 RMS jitter with various ring sizes

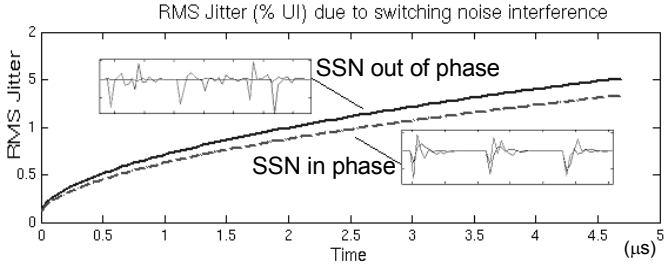

Fig. 7 Jitter due to 2 switching noise sources with (solid line) and without (dotted line) phase differences.

4.3 Implementation

In practice, the periodic switching noise $\boldsymbol{f}(t)$ and PLL sensitivity profile $g(t)$ are obtained through numerical simulations with time step t_s. Let $Q = T_g/t_s$, then (11) becomes

$$\phi[i] = \sum_{u=0}^{iQ-1} \varphi(ut_s) . \qquad (12)$$

The *root mean square* (RMS) timing jitter at the i^{th} transition is

$$\sqrt{\langle \Delta t^2(0, iT_g)\rangle} = \frac{T_g}{2\pi}\sqrt{\left[\sum_{r=0}^{\left\lfloor \frac{Q-1}{N} \right\rfloor} \sum_{m=0}^{P-1} \boldsymbol{A}'^2_{m,r}\xi^2_{m,r}(i)\right]\sigma_c^2} , \qquad (13)$$

where $\boldsymbol{A}'_{m,r} = NH_m\boldsymbol{F}_m G_{rN}$, $\xi_{m,r}(i) = \frac{1-e^{j2\pi miQ/P}}{1-e^{j2\pi(rN/Q+m/P)}}$ and σ_c^2 is the variance of Gaussian random variable $\boldsymbol{c}$. Refer to Subsection *7.3* for its derivation details of (13). In particular, the term $\exp(j2\pi mkQ/P)$ reflects the harmonic interactions between the VCO and SSN. (13) provides an efficient analytical model for statistical analysis over various coupling parasitics, spectra of SSN and PLL jitter sensitivities.

5. EXPERIMENTAL RESULTS

In this section, we demonstrate how cyclostationary SSN interference affects VCO jitter using the proposed model. Its efficiency will also be shown next. To compare the number of delay elements in a RO towards its jitter performance, Fig. 6 shows the statistics of RMS jitter accumulated after 30 oscillation cycles with different ring sizes using differential stages for 50 trials. Transition delay for each stage is adjusted so that the VCO output frequency is unchanged. As the number of stage n varies, the SSN is 'sampled' at n regular intervals in each VCO period. The

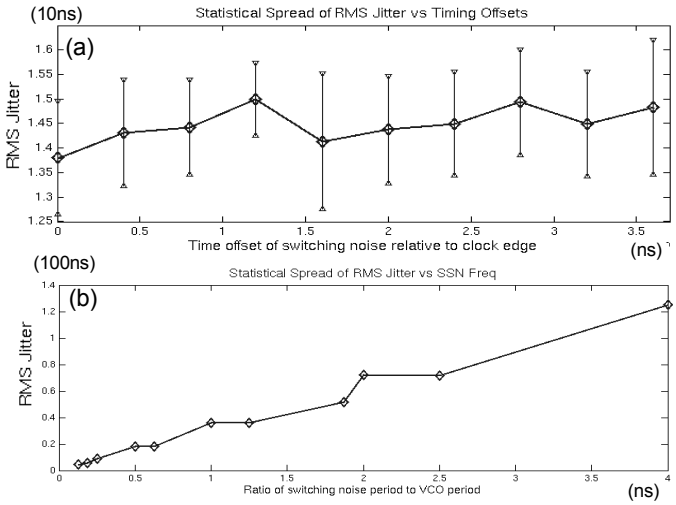

Fig. 8 RMS jitter for various (a) phase, and (b) frequency differences between clock signal and switching logic

mean RMS jitter are denoted by markers, while the vertical bars indicate the $\pm 1\sigma$ spread of the trials. Ring size determines the periodicity and number of super-imposed time-varying noise sensitivity functions. In this case, the 9-stage ring results in the best jitter performance in relation to the statistical characteristics of the SSN model.

In Fig. 7, the jitter due to two SSN sources of the same switching frequency with 0 and π relative phase differences are compared. They model SSN interference in SoCs coming from different clock domains. The result indicates jitter variations depending on the timing offset of multiple SSN sources, whether the noise peaks are out of phase or in phase among others. This enables the relative phase and frequency difference among multiple clock domains in SoCs to be adjusted to minimize their impact. The relative phase among the VCO and the SSN sources also affect the jitter performance. Showing one sweep of a complete VCO period, Fig. 8 examines the jitter performance with various timing differences of SSN sources relative to the VCO transitions.

Table 1 compares the efficiency of obtaining jitter performances via (13) and the Cadence Spectre circuit simulation of a VCO. An actively switching combinational logic circuit is connected to the VCO through substrate parasitics. Spectre is configured to use the "*moderate*" time step control, and the temperature parameters (*temp*, *tnom*) in device models are set to near 0*K* in order to suppress temperature-dependent instrinsic noise sources. Run time of the algorithm is shorter than that of the simulator, especially for long elapsed time. The majority of saved computation time stems from our compact noise models and the analytic SSN-induced jitter equation. The discrepancies can be attributed to numerical error and the stochastic nature of the solutions. Limited time resolution in Spectre analyses, and the linear approximation of jitter sensitivities and other sources of error.

The jitter performance for CMOS inverters (CIs) and differential amplifiers (DAs) implementations with various delay element types are expressed in Table 2. Note that for an *N*-stage RO, there are 2*N* *n*MOS transitions per period in DAs oscillators and *N* *n*MOS and *p*MOS transitions for CI oscillators. *n*-wells are more insulated from SSN coupling than the bulk substrate due to junction capacitance. Hence the CI RO is more robust against jitter *induced by SSN*. Nonetheless, Table 2 compares only the theoretical SSN-induced jitter component, other jitter components are needed to be considered to compare the overall jitter for different RO types, such as in [6,7].

Table 1: Performance comparison between our method and Spectre simulator for computing SSN jitter for a 97MHz VCO

VCO Periods	8	16	64	256
Run time (s) (*Our Method*)	0.5051	0.5114	0.6086	0.9444
Jitter (ps) (*Our Method*)	92.93	97.67	241.5	440.9
Run time (s) (*Spectre*)	153.74	332.8	>30min	>30min
Jitter (*ps*) (*Spectre*)	119.2	162.4	--	--

Table 2: Substrate coupling-induced jitter statistics for 7-stage ring oscillators after 50 periods over 20 trials

Delay Element Type	Frequency (MHz)	Slew Rate (MV/s)	Mean RMS Jitter (ps)	Mean RMS Jitter (UI)
CMOS Inverters	237.9	2497	30.98	0.99%
Single-Ended Amplifiers	104.8	587.3	194.3	4.8%
***n*MOS Differential Amplifiers**	156.7	160.9	184.2	4.6%

6. CONCLUSIONS

Traditional PLL jitter analysis accounts only for the impact of stationary device noise sources. As the PLLs in SoCs are constantly perturbed by SSN, an algorithm for cyclostationary noise-induced jitter analysis is presented to model and compute the dynamical interactions between the SSN interference and the PLL. It provides a preliminary but effective strategy to compare large number of jitter performances that are otherwise too expensive to simulate. This provides guidance for a parasitic-aware PLL design, guard rings assignments, as well as the floorplanning of SoCs. Performance for multiple PLLs implemented in SoC can thus be optimized at the early stage of the design cycle.

7. APPENDIX

7.1 Karhunen-Loeve Basis Functions Derivation

Suppose a transient SSN waveform $x(t)$ is given for M clock periods T, and let there be P fixed time steps in each period. $x(t)$ can then be written as a sequence of M vectors $\boldsymbol{x}_i(t)$, $0 \le i \le M-1$, $iT \le t \le (i+1)T$, each denotes the SSN sequence for 1 period. Consider its $P \times P$ autocorrelation matrix

$$R = \sum_{i=1}^{M} E[\boldsymbol{x}_i \boldsymbol{x}_i^t]. \qquad (14)$$

Since the KL expansion for the SSN samples is

$$\boldsymbol{x}_i = \sum_{j=1}^{P} c_{ij}\psi_j(t) = \Psi \boldsymbol{c}_i, \quad (15)$$

Thus $R = \Psi diag(\lambda_1, \ldots, \lambda_P)\Psi^t$ where $\lambda_i = \sum_{i=1}^{M} E[\boldsymbol{c}_i \boldsymbol{c}_i^t]$, or

$$R\psi_j = \lambda_i \psi_j. \quad (16)$$

Hence KL expansion basis $\{\psi_j(t)\}$ can be found by solving for the eigenvalues of the M-averaged autocorrelation matrix of $\boldsymbol{x}_i$:

1. Form R from SSN samples $\{\boldsymbol{x}_1(t), \ldots, \boldsymbol{x}_M(t)\}$.
2. Obtain eigenvalues $(\lambda_1, \ldots, \lambda_P)$ of R.
3. Sort eigenvalues $|\lambda_1| \geq |\lambda_2| \geq \ldots \geq |\lambda_P|$.
4. Solve $(R - I\lambda_j)\phi_j = \boldsymbol{0}$ for $j = 1, \ldots, P$.

Suppose the estimated *probability density function* over M sample periods is Gaussian. Since $[\boldsymbol{x}_1(t), \ldots, \boldsymbol{x}_M(t)] = \Psi(t)[\boldsymbol{c}_1, \ldots, \boldsymbol{c}_M]$, we compute P Gaussian distributions

$$f_{\boldsymbol{c}_i}(c_j) = \aleph(\mu_j, \sigma_j^2) \quad j = 1, \ldots, P, \quad (17)$$

where $\mu_j = \frac{1}{M-1}\sum_{i=1}^{M} c_{ij}$ and $\sigma_j^2 = \frac{1}{M-1}\sum_{i=1}^{M}(c_{ij} - \mu_j)^2$.

7.2 Derivation of (10)

We expanded the spectra of $\boldsymbol{f}(t)$ in (6) to obtain (9), repeated here as

$$x(t) = \boldsymbol{e}^t \Psi \boldsymbol{c} = \sum_{m=-\infty}^{\infty}\sum_{i=1}^{N} \Psi_{im} c_i \exp\left(\frac{j2\pi m\tau}{T_f}\right), \quad (18)$$

where $\Psi_{im} = 1/T_f \int_{T_f} \psi_i(\tau)\exp(j2\pi m\tau/T_f)d\tau$, and T_f is the SSN period. Let $\boldsymbol{F}_m = [\Psi_{1m}, \Psi_{2m}, \ldots, \Psi_{Nm}]$, the instantaneous phase lag

$$\varphi(t) = \sum_{l=0}^{N-1}\sum_{m,n=-\infty}^{\infty} \boldsymbol{F}_m \boldsymbol{c} G_n \exp\left(j2\pi n\left(\frac{t}{T_g} - \frac{l}{N}\right)\right) \cdot \int_{-\infty}^{t} h(t-\tau)\exp\left(\frac{j2\pi m\tau}{T_f}\right)d\tau \quad . \quad (19)$$

The integral in (19) can be written as

$$\exp\left(\frac{j2\pi mt}{T_f}\right)\int_0^{\infty} h(\sigma)\exp\left(\frac{-j2\pi m\sigma}{T_f}\right)d\sigma, \quad (20)$$

where $\sigma = t - \tau$, $d\sigma = -d\tau$ and $\tau:(-\infty, t) \rightarrow \sigma:(\infty, 0)$. Note that the integral in (20) is the unilateral Fourier transform $H(j2\pi m/T_f)$ of $h(t)$. Substituting (20) in (19),

$$\varphi(t) = \sum_{l=0}^{N-1}\sum_{m,n=-\infty}^{\infty} \boldsymbol{F}_m \boldsymbol{c} H_m G_n \exp\left(j2\pi t\left(\frac{n}{T_g} + \frac{m}{T_f}\right)\right)\exp\left(\frac{-j2\pi nl}{N}\right), \quad (21)$$

where $H_m = H(j2\pi m/T_f)$.

As $\sum_{l=0}^{N-1}\exp\left(\frac{-j2\pi nl}{N}\right) = \begin{cases} N & \text{if } n = rN,\ r \text{ integer} \\ 0 & \text{otherwise} \end{cases}$, we have

$$\varphi(t) = \sum_{m,r=-\infty}^{\infty} A_{m,r}\exp\left(j2\pi t\left(\frac{rN}{T_g} + \frac{m}{T_f}\right)\right), \; A_{m,r} = NH_m \boldsymbol{F}_m \boldsymbol{c} G_{rN}. \quad (22)$$

7.3 Derivation of (13)

Assume that f, g share common simulation time step t_s such that $f[i] = f(it_s)$ and $g[i] = g(it_s)$. Their spectra contain *finite* number of Fourier components $\boldsymbol{F}_m$, $m = 0, 1, \ldots, P-1$, and G_n, $n = 0, 1, \ldots, Q-1$, where $P = T_f/t_s$ and $Q = T_g/t_s$ are natural numbers. The accumulated phase noise is a partial sum (12) of the geometric time series (22). Hence

$$\phi[i] = \sum_{r=0}^{\left\lfloor\frac{Q-1}{N}\right\rfloor}\sum_{m=0}^{P-1} A_{m,r}\xi_{m,r}(i), \quad (23)$$

where $\boldsymbol{A}'_{m,r} = NH_m \boldsymbol{F}_m G_{rN}$ and $\xi_{m,r}(i) = \frac{1 - e^{j2\pi miQ/P}}{1 - e^{j2\pi(rN/Q + m/P)}}$. The mean square phase noise is then

$$\langle \phi^2[i] \rangle = \left[\sum_{r=0}^{\left\lfloor\frac{Q-1}{N}\right\rfloor}\sum_{m=0}^{P-1} \boldsymbol{A}'^2_{m,r}\xi^2{}_{m,r}(i)\right]\sigma_{\boldsymbol{c}}^2, \quad (24)$$

where $\sigma_{\boldsymbol{c}}^2$ is the variance of Gaussian random variable $\boldsymbol{c}$.

8. REFERENCES

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